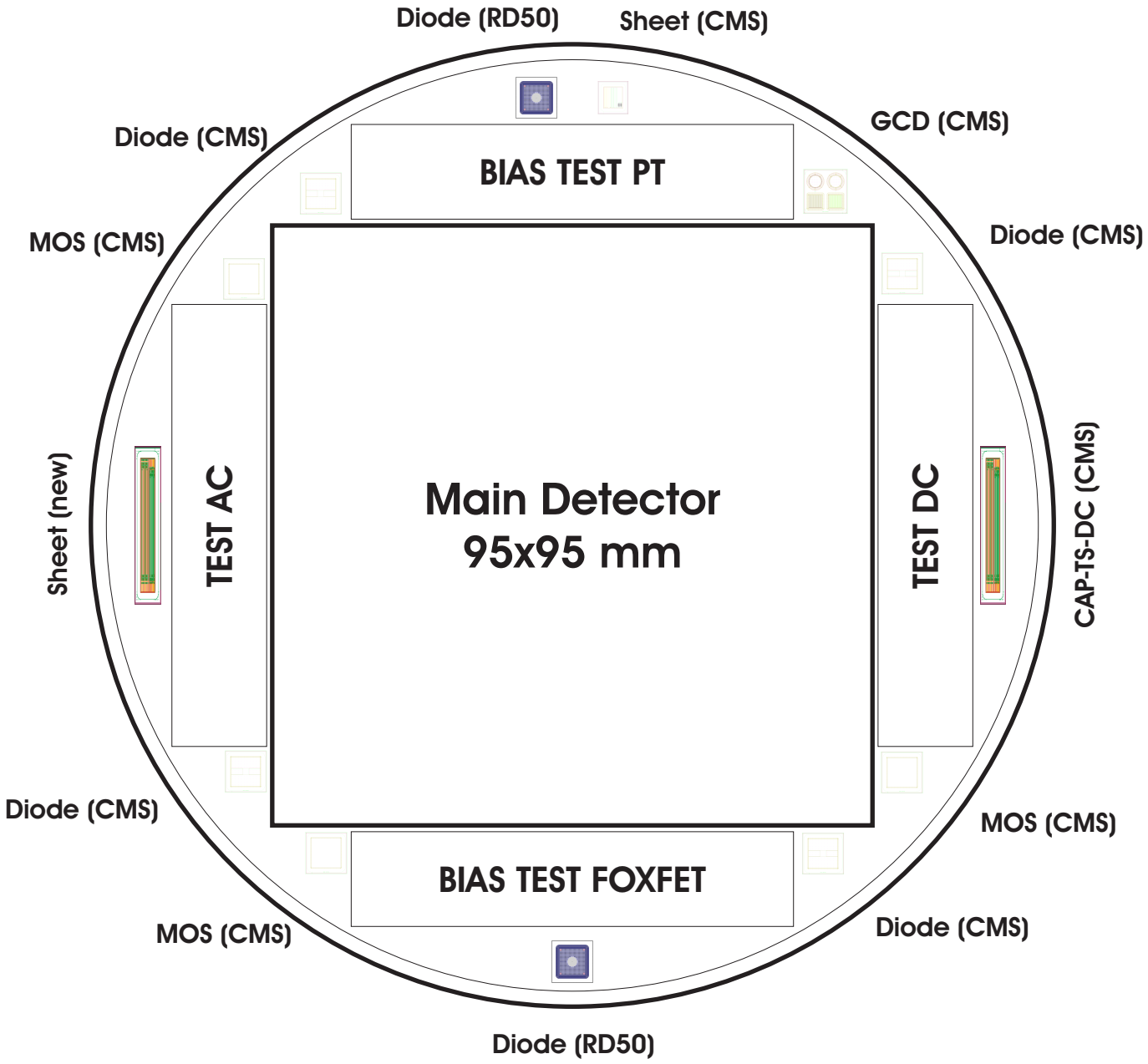
Wafer Design



Main Detector ("Standard Type")

single-sided AC coupled SSD

Sensor size: approx. 95 x 95 mm^2 (exact size based on number of strips and area needed for bias ring and guard ring)

Wafer thickness: approx. 320 μm

Resistivity: such that depletion voltage: 50 V $< V_{depl} <$ 100 Volt

Leakage current: $<$10 μA per sensor

Biasing scheme: poly-Silicon Resistor with 20 M (±5 M

Number of strips: 1792
Strip pitch: 50 μm pitch, no intermediate strips
Strip width: 12.5 μm

Dielectric Structure: Oxide (SiO_2) + Nitride (Si_3N_4) between p^+ and aluminum strips. Thicknesses like for CMS

2 bond pads on each side of the strip (CMS size)
1 probe pad on each side of the strip (contact to p^+)

Additional sensors ("Alignment type"):

single-sided AC coupled SSD (5 pcs.)

Same specifications like above ("Standard Type") but with these modifications:
- Polished backside
- Hole with approx. 1 cm diameter on backside aluminum (CMS type)

TEST AC

Length: 70 mm long strips
Width: 15 mm

Biasing Scheme: poly-Silicon resistors (same as main detector

256 Strips with 50 μm pitch (readout strips)
Different strip widths and intermediate strips according to this table:

strips	strip width [μm]	intermediate strips
16	5	no
16	10	no
16	12.5	no
16	15	no
16	20	no
16	25	no
16	5	single
16	7.5	single
16	10	single
16	12.5	single
16	15	single
16	17.5	single
16	5	double
16	7.5	double
16	10	double
16	12.5	double
sum: 256		

Intermediate strips: p^+ only, no aluminum

2 bond pads on each side (same as main detector)
1 probe pad of readout strip on each side (contact to p^+)
1 probe pad to each intermediate strip (contact to p^+)

Dielectric structure: same as main detector

TEST DC

Same layout as **TEST AC**, but:

Dielectric structure: DC coupled (contact between p^+ and aluminum)

BIAS TEST PT

DC coupled (contact between p^+ and aluminum)
Length: 70 mm long strips
Width: 15 mm

Total number of strips: 256 readout strips
Strip pitch: 50 μm pitch
Strip width: 12.5 μm
Intermediate stip: none

Biasing scheme: punch-through (PT)

2 bond pads on each side (like on main detector)

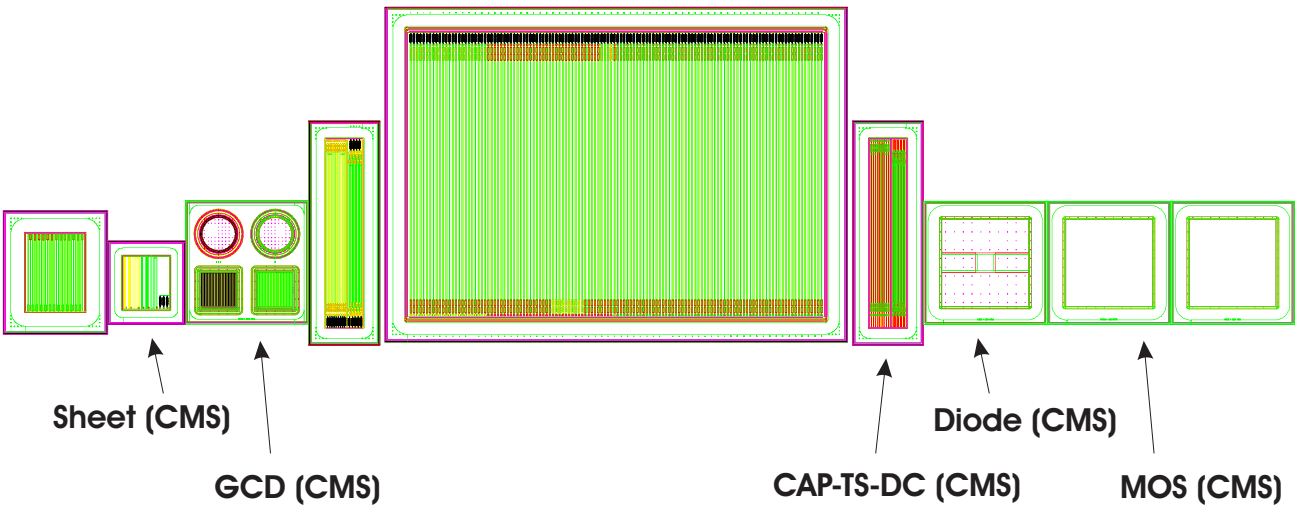
BIAS TEST FOXFET

Same Layout as BIAS TEST PT, but:
Biasing scheme: FOXFET (with additional gate voltage ring)

Small Test Structures

Small test structures at the wafer:

- **Sheet (CMS)** : layout from CMS cutoff (see below)
- **GCD:** Gate Controlled Diode layout from CMS cutoff
- **CAP-TS-DC**: layout from CMS cutoff
- **Diode (CMS):** layout from CMS cutoff
- **Mos:** layout from CMS cutoff



Different test structures compared to CMS cutoff:

- **Sheet (new)**: modified version in respect to CMS cutoff.
  - Length: 25 mm, Width 4 mm.
  - Three aluminum lines, each 75 mm long, width=10, 20, 50 μm
  - three p+ lines, each 75 mm long, width=10, 20, 50 μm
  - Pad size: 150 μm wide, 1000 μm long

- **Diode (Rd50)**: Diode with Multi-guard-ring structure (GDS file available)